DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms
Revision Notes:
Revision C Changes:
1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
2) Reduce R24, 33, 68, 42 from 100K to 10K
3) Add pullup resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
4) Fuse (PTC) recommendation note for R30, 12V input
5) Connect U6 to USB 2
6) Connect U3.16 to U3.4
7) Connect J2.10 to U3.4
8) Add 4.75K resistors to 4.99K
9) Add rubber foot to B06
10) Add staple point via for 32 USB connector.

Revision D Changes (no production):
1) Moved mechanical information to back page.

Revision E Changes (no production):
1) Replaced U1 from MAX13035EETE+ to TI TXS02612ZQSR part
2) Added Sheet 11.
3) Added mechanical information to back page.

Revision F Changes:
1) Changed USB UART default power to bus power. Attach VBUS/L power net to U2.7 REGIN pin. Disconnect Vdd pin from +5.3V.
2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
3) Added D9, D11, J77, R97, R98 to allow user to configure USB Bus or Self power mode.
4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
5) Added D12 PolyZen (PTC+Zen) USB UART protection component as configurable option.
6) Added R99 0 ohm resistor for D12 bypass (default).
7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
8) Revised notes (above).
9) 28 Jan 14: Updated 1336 OTG configuration notes.
10) 10 Dec 14: Updated F02 notes on about 3.

Mechanicals:

PCB Mounting Holes

Fansink Mounting Holes